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EXAMINER	
SMOOT, STEPHEN W	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,836	WEIMER ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7-3-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to application papers filed on 03 July 2003.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign mentioned in the description:

824 in Fig. 9 (see paragraph [0050]).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 9-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A broad range or limitation together with a narrow range or limitation that falls within the broad range or limitation (in the same claim) is considered indefinite, since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. Note the explanation given by the Board of Patent Appeals and Interferences in *Ex parte Wu*, 10 USPQ2d 2031, 2033 (Bd. Pat. App. & Inter. 1989), as to where broad language is followed by "such as" and then narrow language. The Board stated that this can render a claim indefinite by raising a question or doubt as to whether the feature introduced by such language is (a) merely exemplary of the remainder of the claim, and therefore not required, or (b) a required feature of the claims. Note also, for example, the decisions of *Ex parte Steigewald*, 131 USPQ 74 (Bd. App. 1961); *Ex parte Hall*, 83 USPQ 38 (Bd. App. 1948); and *Ex parte Hasche*, 86 USPQ 481 (Bd. App. 1949).

In the present instance, claim 9 recites the broad recitation “the one or more silicon-containing compounds are halogenated silicon compounds” (see claim 9, lines 1-2), and the claim also recites “the one or more silicon-containing compounds consist of silicon and chlorine” (see claim 6, lines 1-2), which is the narrower statement of the limitation.

Claims 10-11 are rejected under 35 U.S.C. 112, second paragraph, because they depend on claim 9.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 3-19, 21-23, 25-28, 34-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka et al. (US 2003/0222318 A1).

Referring to paragraphs [0177] to [0182], Tanaka et al. (US 2003/0222318 A1) disclose a method of forming a silicon nitride film using a silicon source that does not contain hydrogen (or its other isotopes) and a nitrogen source that contains deuterium. Examples of the silicon source are TCS - tetrachlorosilane (i.e. $SiCl_4$) and HCD - hexachlorodisilane (i.e. Si_2Cl_6) and an example of the nitrogen source is ND_3. These are all of the limitations set forth in claims 1, 5-8, 12-13, 16-18 of the applicant's invention.

The silicon nitride film containing deuterium can be applied to other embodiments disclosed by Tanaka et al. (US 2003/0222318 A1) and, further, can be substituted for a stacked structure comprising lower and upper silicon nitride films disclosed in these other embodiments (see paragraph [0181]).

Regarding claims 3-4, 9-11, the first embodiment disclosed by Tanaka et al. (US 2003/0222318 A1) includes an SiN film (110) formed by low pressure chemical vapor deposition (LP-CVD) at a temperature of 700 degrees C, a pressure of 0.5 Torr, a TCS flow rate of 100 sccm, and an ammonia flow rate of 1000 sccm (i.e. the volume ratio of ammonia to TCS is 10:1) (see Fig. 5 and paragraphs [0063], [0074]).

Regarding claims 14-15, the first embodiment disclosed by Tanaka et al. (US 2003/0222318 A1) includes the SiN film (110) in direct contact with a gate electrode (104, 105, 106) that comprises an amorphous silicon film (104) that can be doped with p-type impurities (see Fig. 5 and paragraph [0062]).

Regarding claims 19, 21-23, 25-28, the first embodiment disclosed by Tanaka et al. (US 2003/0222318 A1) includes a silicon substrate (101) with a silicon oxynitride gate insulating film (103) in direct contact with the silicon substrate (101), a gate electrode (104, 105, 106) that comprises an amorphous silicon film (104) that can be doped with p-type impurities formed over the gate insulating film (103), lower and upper SiN films (107, 108) formed over and in direct contact with the gate electrode (104, 105, 106), the lower and upper SiN films (107, 108) and gate electrode (104, 105, 106) are formed into a gate stack by dry etching, and the SiN film (110) lines the sidewalls of the gate stack (see Figs. 1-5 and paragraphs [0061] to [0076]).

Regarding claims 34-42, the first embodiment disclosed by Tanaka et al. (US 2003/0222318 A1) includes a gate electrode (104, 105, 106) formed over a silicon substrate (101), the SiN film (110) lines the sidewalls of the gate electrode (104, 105, 106), and the SiN film is dry etched to selectively leave the SiN film (110) around the gate electrode (see Figs. 4-5 and paragraphs [0062], [0074]).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 2003/0222318 A1) as applied to claim 19 above, and further in view of Wolf and Tauber.

As shown above, Tanaka et al. (US 2003/0222318 A1) anticipate claim 19 of the applicant's invention. However, Tanaka et al. (US 2003/0222318 A1) do not expressly teach or suggest using monocrystalline silicon as their silicon substrate, which is the further limitation to claim 19 set forth in claim 24 of the applicant's invention. Wolf and Tauber teach that single crystal silicon substrates are used for VLSI fabrication (see page 5, fourth full paragraph).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Tanaka et al. (US 2003/0222318 A1) with those of Wolf and Tauber in order to use single crystal silicon substrates as taught by Wolf and Tauber. Wolf and Tauber recognize that single crystal silicon has the advantage of increased minority carrier lifetimes (see page 5, fourth full paragraph).

8. Claims 1-14, 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eklund (US 6,114,734) in view of M. Tanaka et al. (2001 VLSI technical paper – from applicant's IDS).

Referring to Figs. 1-4 and column 2, line 33 to column 3, line 46, Eklund discloses a method of forming a transistor structure that includes the following features:

- A gate oxide (210) is formed over a semiconductor active area (200) of a wafer;
- A gate electrode (220) is formed over the gate oxide (210);
- In an alternative embodiment, a deuterated nitride cap (240 in Fig. 4) is formed over the gate electrode (220) (also see column 3, lines 55-63);
- Deuterated nitride spacers (230) are formed on the sidewalls of the gate oxide (210), the gate electrode (220), and the deuterated nitride cap (240) as shown in Fig. 4;
- Source/drain regions (260) are formed adjacent to the gate electrode (220) sidewalls as shown in Fig. 3;

- A deuterated silicon nitride layer (310) is deposited over the deuterated nitride cap (240) and the deuterated nitride spacers (230);
- The deuterated nitride is formed using dichlorosilane (SiH_2Cl_2) and deuterated ammonia (ND_3) gases at a pressure of 200 mTorr (0.2 Torr) and preferably at a temperature of 750 degrees C, which implies a chemical vapor deposition process;
- The ammonia to dichlorosilane ratio is 10:1; and
- In an alternative embodiment, deuterated silicon oxynitride may be used as the spacer material (also see column 5, lines 42-45).

These are limitations set forth in claims 1-5, 8-14, 16-18 of the applicant's invention.

However, Eklund lacks the following claimed features of the applicant's invention:

- The step of forming the deuterated nitrides by using a halogenated silicon compound that does not contain hydrogen isotopes (a limitation of claims 1, 16); and
- Using $SiCl_4$ or Si_2Cl_6 as the halogenated silicon compound (a limitation of claims 6-7, 17).

M. Tanaka et al. (2001 VLSI technical paper – from applicant's IDS) teach the formation of silicon nitride films by substituting tetrachlorosilane ($SiCl_4$) for dichlorosilane (SiH_2Cl_2) (see page 123).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method of Eklund by substituting tetrachlorosilane ($SiCl_4$) for dichlorosilane (SiH_2Cl_2) as taught by M. Tanaka et al. (2001

VLSI technical paper – from applicant's IDS). M. Tanaka et al. (2001 VLSI technical paper – from applicant's IDS) recognize that the use of tetrachlorosilane suppresses boron penetration in the silicon nitride film and thereby improves the performance of DRAMs (see page 123, Conclusion).

9. Claims 19-25, 27-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eklund (US 6,114,734) in view of Wolf and Tauber, M. Tanaka et al. (2001 VLSI technical paper – from applicant's IDS), and Yoo et al. (US 6,271,125 B1).

Referring to Figs. 1-4 and column 2, line 33 to column 3, line 46, Eklund discloses a method of forming a transistor structure that includes the following features:

- A gate oxide (210) is formed over a semiconductor active area (200) of a wafer;
- A gate electrode (220) is formed over the gate oxide (210);
- In an alternative embodiment, a deuterated nitride cap (240 in Fig. 4) is formed over the gate electrode (220) (also see column 3, lines 55-63);
- Deuterated nitride spacers (230) are formed on the sidewalls of the gate oxide (210), the gate electrode (220), and the deuterated nitride cap (240) as shown in Fig. 4;
- Source/drain regions (260) are formed adjacent to the gate electrode (220) sidewalls as shown in Fig. 3;
- A deuterated silicon nitride layer (310) is deposited over the deuterated nitride cap (240) and the deuterated nitride spacers (230);

- The deuterated nitride is formed using dichlorosilane (SiH_2Cl_2) and deuterated ammonia (ND_3) gases at a pressure of 200 mTorr (0.2 Torr) and preferably at a temperature of 750 degrees C, which implies a chemical vapor deposition process;
- After fabrication of the transistor structure is completed, the structure is sintered for 30 to 120 minutes at a temperature of 350 to 480 degrees C; and
- In an alternative embodiment, deuterated silicon oxynitride may be used as the spacer material (also see column 5, lines 42-45).

These are limitations set forth in claims 19-21, 25, 30-31 of the applicant's invention. However, Eklund lacks the following claimed features of the applicant's invention:

- The semiconductor active area comprising silicon (a limitation of claim 19);
- The step of forming the deuterated nitrides by using a halogenated silicon compound that does not contain hydrogen isotopes (a limitation of claims 19, 28-29);
- Using $SiCl_4$ or Si_2Cl_6 as the halogenated silicon compound (a limitation of claims 22-23);
- The semiconductor active area being monocrystalline silicon (the limitation of claim 24);
- The step of etching the electrically conductive material (e.g. a gate electrode) and the deuterated silicon nitride-containing material (e.g. a deuterated cap) to form a wordline (a limitation of claim 27); and

- Incorporating the transistor into a DRAM cell and incorporating the DRAM cell into an electronic system (the limitations of claims 32-33).

Wolf and Tauber teach that single crystal silicon substrates are used for VLSI fabrication (see page 5, fourth full paragraph). M. Tanaka et al. (2001 VLSI technical paper – from applicant's IDS) teach the formation of silicon nitride films by substituting tetrachlorosilane ($SiCl_4$) for dichlorosilane (SiH_2Cl_2) (see page 123). Yoo et al. teach the formation of transfer gate transistors by anisotropically etching a gate stack that includes a silicon nitride layer and a polycide gate electrode (see column 5, line 38-67). Yoo et al. further teach the use of their transistors in an embedded DRAM that is integrated with logic devices (see column 1, lines 52-56).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Eklund with those of Wolf and Tauber in order to use single crystal silicon substrates as taught by Wolf and Tauber for the semiconductor active area of Eklund. It further would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method of Eklund by substituting tetrachlorosilane ($SiCl_4$) for dichlorosilane (SiH_2Cl_2) as taught by M. Tanaka et al. (2001 VLSI technical paper – from applicant's IDS). It also would have been obvious to a person of ordinary skill in the art at the time the invention was made to form wordlines by etching a gate stack as taught by Yoo et al. and by using the transfer gate transistors in an embedded DRAM that is integrated with logic devices as taught by Yoo et al.

Wolf and Tauber recognize that single crystal silicon has the advantage of increased minority carrier lifetimes (see page 5, fourth full paragraph). M. Tanaka et al. (2001 VLSI technical paper – from applicant's IDS) recognize that the use of tetrachlorosilane suppresses boron penetration in the silicon nitride film and thereby improves the performance of DRAMs (see page 123, Conclusion). The teachings of Yoo et al. show that it is known in the art to form transfer gate transistors by etching gate stacks and to utilize the transfer gate transistors in an embedded DRAM that is integrated with logic devices.

10. Claims 34-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eklund (US 6,114,734) in view of M. Tanaka et al. (2001 VLSI technical paper – from applicant's IDS) and Yoo et al. (US 6,271,125 B1).

Referring to Figs. 1-4 and column 2, line 33 to column 3, line 46, Eklund discloses a method of forming a transistor structure that includes the following features:

- A gate oxide (210) is formed over a semiconductor active area (200) of a wafer;
- A gate electrode (220) is formed over the gate oxide (210);
- In an alternative embodiment, a deuterated nitride cap (240 in Fig. 4) is formed over the gate electrode (220) (also see column 3, lines 55-63);
- Deuterated nitride spacers (230) are formed on the sidewalls of the gate oxide (210), the gate electrode (220), and the deuterated nitride cap (240) as shown in Fig. 4;

- Source/drain regions (260) are formed adjacent to the gate electrode (220) sidewalls as shown in Fig. 3;
- A deuterated silicon nitride layer (310) is deposited over the deuterated nitride cap (240) and the deuterated nitride spacers (230);
- The deuterated nitride is formed using dichlorosilane (SiH_2Cl_2) and deuterated ammonia (ND_3) gases at a pressure of 200 mTorr (0.2 Torr), which implies a chemical vapor deposition process;
- After fabrication of the transistor structure is completed, the structure is sintered for 30 to 120 minutes at a temperature of 350 to 480 degrees C; and
- In an alternative embodiment, deuterated silicon oxynitride may be used as the spacer material (also see column 5, lines 42-45).

These are limitations set forth in claims 34-37, 40-43, 45-49, 52-55 of the applicant's invention.

However, Eklund lacks the following claimed features of the applicant's invention:

- The step of anisotropically etching to form the spacers (a limitation of claims 34, 43);
- The step of implanting dopant to form the source/drain regions (a limitation of claim 43);
- The step of forming the deuterated nitrides by using a halogenated silicon compound that does not contain hydrogen isotopes (a limitation of claims 34, 43, 45-47);

- Using $SiCl_4$ or Si_2Cl_6 as the halogenated silicon compound (a limitation of claims 38-39, 50-51);
- The step of depositing a deuterated silicon oxynitride-containing material over the gate stack and over the spacers (the limitation of claim 44); and
- Incorporating the transistor into a DRAM cell and incorporating the DRAM cell into an electronic system (the limitations of claims 56-57).

M. Tanaka et al. (2001 VLSI technical paper – from applicant's IDS) teach the formation of silicon nitride films by substituting tetrachlorosilane ($SiCl_4$) for dichlorosilane (SiH_2Cl_2) (see page 123). Yoo et al. teach the formation of silicon nitride spacers on gate structures by depositing a silicon nitride layer followed by anisotropically etching the layer to form the spacers and the formation of source/drain regions by ion implantation (see column 4, line 66 to column 5, line 18). The alternate embodiment taught by Eklund of substituting deuterated silicon oxynitride for the deuterated nitride spacers (see column 5, lines 42-45) suggests that deuterated silicon oxynitride can be substituted for other deuterated nitride components in Eklund's transistor structure. Yoo et al. further teach the use of their transistors in an embedded DRAM that is integrated with logic devices (see column 1, lines 52-56).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method of Eklund by substituting tetrachlorosilane ($SiCl_4$) for dichlorosilane (SiH_2Cl_2) as taught by M. Tanaka et al. (2001 VLSI technical paper – from applicant's IDS), by anisotropically etching a silicon nitride layer to form the spacers as taught by Yoo et al., by ion implanting to form the

source/drain regions as taught by Yoo et al., by substituting deuterated silicon oxynitride for the deuterated silicon nitride layer (310) of Eklund as suggested by Eklund, and by using the transistors in an embedded DRAM that is integrated with logic devices as taught by Yoo et al.

M. Tanaka et al. (2001 VLSI technical paper – from applicant's IDS) recognize that the use of tetrachlorosilane suppresses boron penetration in the silicon nitride film and thereby improves the performance of DRAMs (see page 123, Conclusion). The teachings of Yoo et al. show that it is known in the art to form silicon nitride spacers by anisotropic etching, to form source/drain diffusion regions by ion implanting p-type or n-type dopants, and to utilize field effect transistors in an embedded DRAM that is integrated with logic devices. The suggestion of Eklund to substitute deuterated silicon oxynitride for deuterated silicon nitride would have the advantage of lowering the dielectric constant of the deposited films and thereby would have the effect of reducing parasitic capacitances in the transistor structures.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lyding et al. and Burnham et al. teach methods that feature forming deuterated silicon nitride layers.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

Stephen W. Smoot
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